Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-10 (Canceled)

Claim 11 (Original): A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer having a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area,

wherein the dummy structures are inactive areas configured to increase the planarity of a metal layer subsequently formed on the dielectric layer;

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the non-recessed area.

Claim 12 (Original): The structure of claim 11, wherein the recessed area has a depth corresponding to a thickness of the metal layer to remain within the recessed area after electropolishing and an offset height corresponding to a distance between a surface of the non-recessed area to be exposed after electropolishing and a surface of the metal layer to remain within the recessed area after electropolishing.

Claim 13 (Original): The structure of claim 12, further comprising removing the exposed non-recessed area to a depth equal to the offset height.

Claim 14 (Original): The structure of claim 13, wherein the offset height is between about 5 nanometers to about 100 nanometers.

Claim 15 (Original): The structure of claim 11, wherein the metal layer is formed by depositing the metal layer.

Claim 16 (Original): The structure of claim 11, wherein the metal layer is formed by electroplating the metal layer.

Claim 17 (Original): The structure of claim 11,

wherein each dummy structure in the plurality has a width,

wherein the metal layer has a thickness,

wherein the thickness is based on the metal layer formed on the non-recessed area, and

wherein a ratio of the width to the thickness is between about 0.1 to about 1.

Claim 18 (Original): The structure of claim 17, wherein the ratio is 0.3.

Claim 19 (Original): The structure of claim 11,

wherein dummy structures in the plurality are spaced apart from each other by a distance,

wherein the metal layer has a thickness,

wherein the thickness is based on the metal layer formed on the non-recessed area, and

wherein a ratio of the distance to the thickness is between about 1 to about 5.

Claim 20 (Original): The stucture of claim 19, wherein the ratio is less than 2.

Claim 21 (Original): The structure of claim 11, further comprising:

a barrier layer formed on the dielectric layer before forming the metal layer.

Claim 22 (Original): The structure of claim 11, further comprising:

a seed layer formed on the dielectric layer before forming the metal layer.

Claim 23 (Original): The structure of claim 11, further comprising:

a cover layer formed on the semiconductor wafer after electropolishing the metal layer.

Claim 24 (Original): The structure of claim 11, wherein the recessed area is a wide trench configured to form an interconnection when filled with the metal layer.

Claim 25 (Original): The structure of claim 11, wherein the recessed area is a large rectangular structure configured to form a pad when filled with the metal layer.

Claim 26 (Original): The structure of claim 25, wherein the exposed non-recessed area is removed beyond a surface of the electropolished metal layer to form a pad that protrudes beyond the dielectric layer to facilitate contact between the pad and a probe used for electrical testing.

Claim 27 (Original): The structure of claim 25, wherein the large rectangular structure has rounded corners.

Claim 28 (Original): The structure of claim 11, wherein the metal layer is copper.

Claim 29 (Original): The structure of claim 11, wherein the plurality of dummy structures includes the same material as the dielectric layer.

Claim 30 (Original): The structure of claim 11, wherein the plurality of dummy structures includes a metal.

Claim 31 (Original): A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer,

wherein the dielectric layer is formed with a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area;

a barrier layer formed to cover the recessed area, the non-recessed area, and the plurality of dummy structures; and

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the barrier layer deposited on the non-recessed area, and wherein the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

Claim 32 (Original): The structure of claim 31, wherein the exposed barrier layer and the non-recessed area of the dielectric layer have even surfaces after the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

Claim 33 (Original): The structure of claim 31, wherein the exposed barrier layer protrudes beyond the non-recessed area after the exposed barrier layer is removed at a first rate and the non-recessed area is removed at a second rate.

Claim 34 (Original): The structure of claim 31, wherein the first rate is equal to the second rate.

Claim 35 (Original): The structure of claim 31, wherein the first rate is lower than the second rate.

Claim 36 (Original): The structure of claim 31, wherein the exposed barrier layer is removed at a third rate and wherein the non-recessed area of the dielectric is removed at a fourth rate.

Claim 37 (Original): The structure of claim 36, wherein the third rate is higher than the fourth rate.

Claim 38 (Original): The structure of claim 37, wherein the fourth rate is zero.

Claim 39 (Original): The structure of claim 36, wherein the fourth rate is higher than the third rate.

Claim 40 (Original): The structure of claim 39, wherein the third rate is zero.

Claim 41 (Original): The structure of claim 36, wherein the first rate is higher than the second rate.

Claim 42 (Original): The structure of claim 36, wherein the exposed barrier layer and the non-recessed area have even surfaces after the exposed barrier layer is removed at a third rate and the non-recessed area is removed at a fourth rate.

Claim 43 (Original): The structure of claim 36, wherein the exposed barrier layer protrudes beyond the non-recessed area after the exposed barrier layer is removed at a third rate and the non-recessed area is removed at a fourth rate.

Claim 44 (New): A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer having a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area,

wherein the dummy structures are inactive areas configured to increase the planarity of a metal layer subsequently formed on the dielectric layer; and

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the non-recessed area, and wherein the metal layer is overpolished to allow the non-recessed area to protrude past a surface of the metal layer in the recessed area.

Claim 45 (New): The structure of claim 44, wherein a portion of the non-recessed area that protrudes past the surface is removed.

Claim 46 (New): The structure of claim 45, wherein the portion of the non-recessed area removed has a thickness of between about 5 to about 100 nanometers.

Claim 47 (New): The structure of claim 44, wherein the metal layer is formed by depositing the metal layer.

Claim 48 (New): The structure of claim 44, wherein the metal layer is formed by electroplating the metal layer.

Claim 49 (New): The structure of claim 44,

wherein the dummy structure has a width,

wherein the metal layer has a thickness,

wherein the thickness is based on the metal layer deposited on the non-recessed area, and

wherein a ratio of the width to the thickness is between about 0.1 to about 1.

Claim 50 (New): The structure of claim 49, wherein the ratio is 0.3.

Claim 51 (New): The structure of claim 44,

wherein the dummy structure is spaced apart from the non-recessed area by a distance,

wherein the metal layer has a thickness,

wherein the thickness is based on the metal layer deposited on the non-recessed area, and

wherein a ratio of the distance to the thickness is between about 1 to about 5.

Claim 52 (New): The structure of claim 44, further comprising a barrier layer formed on the dielectric layer before the metal layer is formed.

Claim 53 (New): The structure of claim 44, further comprising a seed layer formed on the dielectric layer before the metal layer is formed.

Claim 54 (New): The structure of claim 44, further comprising a cover layer formed on the semiconductor wafer after the metal layer is electropolished.

Claim 55 (New): The structure of claim 44, wherein the recessed area is a wide trench configured to form an interconnection when filled with the metal layer.

Claim 56 (New): The structure of claim 44, wherein the recessed area is a large rectangular structure configured to form a pad when filled with the metal layer.

Claim 57 (New): The structure of claim 56, wherein the exposed non-recessed area beyond the surface of the metal layer is removed to form a pad that protrudes beyond the dielectric layer to facilitate contact between the pad and a probe used for electrical testing.

Claim 58 (New): The structure of claim 44, wherein the metal layer is copper.

Claim 59 (New): The structure of claim 45, wherein the dummy structure includes the same material as the dielectric layer.

Claim 60 (New): The structure of claim 44, wherein the dummy structure includes a metal.